Remarks

The Office Action dated November 27, 2009 notes that the drawings and the specification are objected to, and the following rejections: claims 1-2, 4-9 and 12-14 stand rejected under 35 U.S.C. § 103(a) over Krakauer (U.S. Patent No. 5,617,283) in view of Chin (U.S. Patent No. 5,430,602); claim 10 stands rejected under 35 U.S.C. § 103(a) over the '283 and '602 references in view of Ker (U.S. Patent Pub. 2002/0050615); claims 11 and 15 stand rejected under 35 U.S.C. § 103(a) over the '283 and '602 references in view of Lai (US Patent Pub. 2003/0235022); claims 1-2, 4-9 and 11-15 stand rejected under 35 U.S.C. § 103(a) over John (U.S. Patent No. 6,522,511) in view of Ker (U.S. Patent No. 6,912,109); and claim 10 stands rejected under 35 U.S.C. § 103(a) over the '615 reference. Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant respectfully traverses the § 103(a) rejections based on the cited Krakauer '283 reference because the '283 reference, either alone or in combination with the other cited references, lacks correspondence to the claimed invention. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including aspects regarding, *e.g.,* a time-delay circuit that includes a resistor and a capacitive device connected in series between a power supply and control inputs of first and second transistors. Because none of the cited references teaches these aspects, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence. As such, the rejections fail.

More specifically, the Office Action acknowledges that the '283 reference does not teach or suggest a time-delay circuit that includes a resistor and a capacitive device connected as in the claimed invention (*see, e.g.,* page 4 of the instant Office Action). The '602 reference, however, also fails to teach such a time-delay circuit. Specifically, the '602 reference does not teach that resistor R2' (and/or resistor R1) are connected in series with MOS diode T1 (*i.e.,* the asserted capacitive device) between pad 110 and the control inputs of any transistors. Instead, the resistor R2' (and/or resistor R1) and MOS diode T1 are connected in series between pad 110 and a ground voltage terminal Vss as shown in Fig. 2 of the '602 reference, with the MOS diode T1 serving as a clamping circuit (*see, e.g.,* Col. 3:38-40). As such, the Office Action fails to cite any reference that teaches the

time-delay circuit of the claimed invention. Applicant respectfully submits that the Office Action has done little more than identify a series connection of a resistor and a MOS diode and then assert that the skilled artisan would place a resistor in series with transistor 42 of the '511 reference when neither of the cited references teach or suggest doing so. Applicant notes that the series connection of a resistor and transistor 42 would not serve as a clamping circuit in the device of the '511 reference, as taught by the '602 reference. Thus, Applicant submits that the Office Action's proposed combination is improperly based on Applicant's disclosure in an improper hindsight reconstruction of the claimed invention. *See, e.g.,* M.P.E.P. § 2142.

Moreover, the cited portions of the '283 reference do not teach that transistor 42 (*i.e.,* the asserted capacitive device) is connected to a power supply, and, in fact, the '283 reference teaches away from connecting transistor 42 to a power supply. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('283) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). The cited teachings of the '283 reference indicate that transistor 42 is connected to signal line 16. In fact, the '283 reference teaches that the embodiment disclosed in Figure 2 eliminates the need for a reference supply voltage (*e.g.,* V_{DD}) to be available for the modulation circuit 40. *See, e.g.*, Col. 4:59-67. As such, the '283 reference teaches away from connecting transistor 42 to a power supply voltage. Applicant previously highlighted the fact that the '283 reference teaches away from connecting transistor 42 to a power supply voltage. In response thereto, the Office Action erroneously asserts that voltage Vpad applied to signal line 16 is a supply voltage. Applicant respectfully submits that such an interpretation is contrary to the definition of a supply voltage as readily understood by one of skill in the art. *See, e.g.,* M.P.E.P. § 2111. In other words, the Office Action's interpretation improperly affords no meaning to the term "supply."

In addition, the Office Action erroneously asserts that the transistor 42 of the '283 reference is a capacitive device. The '283 reference directly contradicts the Office Action's assertion and expressly states that transistor 42 is "a high impedance resistor 42." *See* Col. 4:22-26. As the Office Action expressly relies upon the transistor 42 of the '283 reference being a capacitive device as the basis for the rejections, the rejections necessarily fail.

In view of the above, the § 103(a) rejections based on the '283 reference are improper and Applicant requests that they be withdrawn.

Applicant respectfully traverses the § 103(a) rejections based on the cited John '511 reference because the '511 reference, either alone or in combination with the other cited references, lacks correspondence to the claimed invention. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including aspects regarding, *e.g.,* a time-delay circuit that includes a resistor and a capacitive device connected in series between a power supply and control inputs of first and second transistors. Because none of the cited references teaches these aspects, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence. As such, the rejections fail.

More specifically, the Office Action acknowledges that the '511 reference does not teach or suggest a time-delay circuit that includes a resistor and a capacitive device connected as in the claimed invention (*see, e.g.,* page 8 of the instant Office Action). The '109 reference, however, also fails to teach such a time-delay circuit. Specifically, the '109 reference does not teach that resistor 44 (or resistor 46) is connected in series with capacitor 42 (*i.e.,* the asserted capacitive device) between terminal VDD and the control inputs of transistors 28 and 30 as is shown in Figure 11. As such, the Office Action fails to cite any reference that teaches the time-delay circuit of the claimed invention.

Moreover, the '511 reference expressly teaches away from the asserted combination with the '109 reference. *See, e.g., KSR* discussed above. In this instance, the Office Action proposes adding the MOS gate 42 capacitor of the '109 reference, which is expressly taught by the '109 reference to be a capacitor (*see, e.g.,* Figures 4 and 11 and Col. 9:60-67), to the ESD detector of the '511 reference. The '511 reference, however, expressly teaches that capacitors should not be used in the '511 reference's ESD detector (*see, e.g.*, Col. 2:14-17 and Col. 3:29-33). In addition, this is one of the

primary objects of the '511 reference and the proposed modification would render the circuit of the '511 reference unsuitable for use in high-speed digital circuitry. *See, e.g.,* M.P.E.P. § 2143.01 ("If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious."). Accordingly, the § 103(a) rejections based on the '511 reference are improper and Applicant requests that they be withdrawn.

In view of the above, the § 103(a) rejections based the '511 reference are improper and Applicant requests that they be withdrawn.

Applicant respectfully traverses the objection to the drawings because the objection relies upon an improper interpretation of the U.S.P.T.O. rules. Specifically, the Office Action erroneously asserts that the drawings "must show every feature of the invention specified in the claims." The definition of a feature is a prominent attribute or aspect of something. In this instance, the specific aspects identified as missing (*i.e.,* a parasitic npn transistor and a thyristor), while possibly relevant, are not prominent attributes or aspects. Rather than limit the cited rule (37 C.F.R. § 1.83(a)) to prominent aspects of the claims, the Office Action appears to take the position that the figures must provide a near word-for-word correspondence to the claims. The Office Action's position, if applied to all cases, would ostensibly require that every patent application contain a near word-for-word replication of all language from the claims into the figures. Moreover, Applicant's position is also supported by a number of U.S. laws, U.S.P.T.O. rules and passages of the M.P.E.P. This support is largely inconsistent with the Office Action's position and will be discussed hereafter.

The Office Action's apparent interpretation of 37 CFR § 1.83(a) is contrary to the U.S.P.T.O. practice, U.S. law and the M.P.E.P. In support of Applicant's position reference is made to 35 USC § 113 and M.P.E.P. § 601.01(f), which indicate that "applicant shall furnish a drawing <u>where necessary</u> for the understanding of the subject matter sought to be patented." The authority for the U.S.P.T.O. to create rules such as 37 C.F.R. § 1.83(a) is derived from 35 USC § 113. Accordingly, 37 C.F.R. § 1.83(a) must be interpreted in light of this law to ensure that the U.S.P.T.O. does not exceed the statutory authority granted by the U.S. Congress. Moreover, M.P.E.P. § 608.02(e)

clarifies how 37 C.F.R. § 1.83(a) should be interpreted and applied by an examiner: "The drawings are objected to under 37 CFR 1.83(a) because they fail to show [1] as described in the specification. Any structural detail *that is essential for a proper understanding of the disclosed invention* should be shown in the drawing." (*emphasis added*). This language is the suggested paragraph for an examiner that wishes to use a 37 C.F.R. § 1.83(a) objection. The Office Action has not used this language, choosing instead to ignore the second half of the suggested language. Accordingly, the objection to the drawings is improper and must be withdrawn.

Regarding the objection to the specification, Applicant disagrees that no explanation/support of the time delay circuit has been provided and/or is required. For example, in connection with Figure 2, the time delay circuit is described as including R and transistor MN1, which provide drive current to the node NET1 as fast as possible. *See also* the tables before the claims section. Applicant notes that the Office Action has maintained this objection despite the fact that Applicant has identified portions of Applicant's specification that provide explanation/support for the time delay circuit. Moreover, the Office Action continues to fail to provide any authority (*e.g.,* from the M.P.E.P. or otherwise) to support the objection to the specification. As such, it is unclear to Applicant upon what basis the Office Action has objected to Applicant's specification and the objection should be removed.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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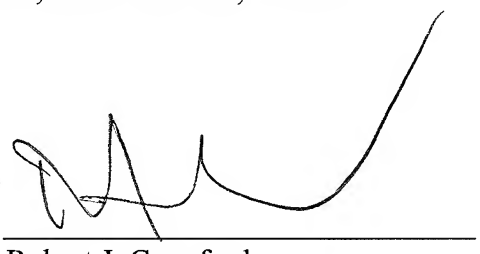
By: 

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